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(54) Title: A COMPOSITION FOR CHEMICAL MECHANICAL POLISHING

(57) Abstract

Use of a complexing agent in a composition comprising amorphous silica for chemical mechanical polishing of a semiconductor substrate, for the purpose of avoiding metal contamination of said semiconductor substrate. A composition for chemical mechanical polishing of semiconductor substrates, which composition contains amorphous silica, ammonium ions, and a sequestering agent, and a method in which such a composition is used to polish a semiconductor substrate.

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A COMPOSITION FOR CHEMICAL MECHANICAL POLISHING

The present invention relates to the use of a complexing agent in a composition for chemical mechanical polishing of a semiconductor substrate, a composition for such chemical mechanical polishing, and a method in which the composition is used.

In the present application the concept of "chemical mechanical polishing", below abbreviated to "polishing" refers - except where otherwise explicitly or implicitly indicated - in addition to polishing processes performed on the semiconductor substrates at the initial phase of the semiconductor wafer production process, also to technically similar processes such as chemical mechanical planarization, which is abbreviated to "planarization" below.

In the present context a "semiconductor" means - except where otherwise explicitly or implicitly indicated - a substance having semiconducting properties as well as a semiconductor component.

Polishing of semiconductor substrates using silica in combination with ammonium is disclosed in e.g. US-A-3,715,842. The silica used has preferably a particle size of less than 100 nm. The polishing composition may contain ammonium, which is referred to as an additional polishing agent. NH_4OH may be present; its contribution to the alkalinity of the silica slurry is briefly discussed. Apart from this the ammonium ions and the NH_4OH are not suggested to have any particular purpose or impact on the polishing process.

The production of semiconductor wafers demands very low impurity levels. In particular metal impurities in the semiconductor substrates may be completely devastating to the substrate. Conventionally this problem has been avoided by using amorphous silica particles having very low metal impurity levels. However, such high purity amorphous silicas have the drawback of being very expensive. It would be desirable to be able to use silica of cheaper grades without running the risk of contamining the semiconductor substrate.

The problem to be solved is thus to provide a way to perform polishing on a semiconductor substrate using a amorphous silica-containing composition that may hold a relatively high amount of metals while reducing or avoiding contamination of the semiconductor substrate.

This problem has now been solved by means of the present invention as defined by the appended claims. More particularly the present invention involves the use of a complexing agent in a composition comprising amorphous silica for polishing of a semi-

conductor substrate, for the purpose of avoiding metal contamination of said semiconductor substrate, whereby the preferred complexing agent is NH_4OH.

The present invention also relates to a composition for polishing of semiconductor substrates, which composition contains amorphous silica, ammonium ions, and a specific type of complexing agent, namely a sequestering agent, preferably a chelating agent. A sequestering agent is a substance that removes a metal ion from a solution system by forming a complex ion that does not have the chemical reactions of the ion that is removed, and a chelating agent is an organic compound in which atoms form more than one co-ordinate bond with metals in solution.

The chelating agent preferably comprises a plurality of substituted acetic acid groups, and may e.g. be chosen from a group comprising ethylenediaminetetraacetic acid (EDTA), diethylenetriaminepentaacetic acid (DTPA), N-(hydroxoethyl)ethylenediamintriacetic acid (HEDTA), and nitrilo triacetic acid (NTA), or a combination thereof.

The amorphous silica is preferably colloidal, i.e. present in a stable dispersion or sol of discrete particles of amorphous silica; this definition is the same as put forward in "The Chemistry of Silica" by Ralph K. Iler, page 312, Wiley & Sons 1979. Preferably, the sizes of the silica particles are less than 200 nm, and suitably within the range from about 5-150 nm.

Furthermore, the present invention relates to a method for polishing of a semiconductor substrate in which a composition containing amorphous silica, ammonium ions, and a sequestering agent, preferably a chelating agent, is used. Again, the chelating agent preferably comprises a plurality of substituted acetic acid groups, and may e.g. be chosen from a group comprising ethylenediaminetetraacetic acid (EDTA), diethylenetriaminepentaacetic acid (DTPA), N-(hydroxoethyl)ethylenediamintriacetic acid (HEDTA), and nitrilo triacetic acid (NTA), or a combination thereof.

According to a specific embodiment of the present invention the method is a method for planarization, which is a process that shows many similarities with polishing, in the more limited scope of that term. The main differences between the methods in fact relate to their purposes, their position in the overall semiconductor wafer production process, and accordingly to the differences between the worked objects: The purpose of the polishing is to prepare the semiconductor substrate for the semiconductor wafer production process by providing it with a suitable surface for that process, whereas the object of the planarization is to accomplish a planarized surface to accommodate further processing. Evidently the polishing takes place prior to the actual semiconductor wafer production process, whereas the planarization occurs during the same. This implies that the workpiece of the polishing is a basically pure semiconductor substrate, whereas the

workpiece of the planarization is a semiconductor substrate with various layers applied upon. The substrate in the planarization may for instance be a silicon substrate with a layer of silicon dioxide on top, whereby one of the main purposes of the planarization is to remove the oxide layer.

The semiconductor substrate may contain any semiconducting substance. Preferably, the semiconducting substance in the substrate is Si, GaAs, InP, Ge, or a combination thereof.

The present invention will now be illustrated by means of a non-limiting example.

Example: A P-doped silicon wafer having a diameter of 200 mm was mounted and held in a polishing head. The polishing head was pushed down onto a polishing pad with a pressure of 0.8 psi. During the polishing, the head and the pad were rotated in opposite directions, the head at a rotating speed of approximately 60 rpm, and the pad at 60 rpm. A composition according to the invention was added as a polishing slurry onto the pad while rotating, containing an ammonium-stabilised silica sol, Nyacol® 601 in an amount of 0.5 percentage by weight, calculated on the composition, and a EDTA in an amount of 7 ppm. Then the wafer was submitted to a standard cleaning procedure in which it was stripped of native oxides in a HF bath, rinsed with deionized water, submerged in a heated and megasonic agitated cleaning bath containing deionized water, hydrogen peroxide, and ammonium hydroxide in a relation of 5:1:1, rinsed with deionized water, then submerged in a heated and megasonic agitated cleaning bath containing a very dilute solution of hydrogen chloride in deionized water, ans finally rinsed with deionized water. As a reference, another silicon wafer of the same kind was polished under the same conditions and cleaning procedure, except that the ammonium-stabilised silica sol was of a high purity grade, Glanzox 3900, and that no EDTA was added to the polishing slurry. After the polishing, the wafer surfaces were analysed by means of Total X-ray Fluorosence (TXRF) and Vapor Phase Decomposition (VPD) + Inductive Coupled Plasma with Mass Spectroscopy (ICP/MS) with respect to a number of metals, indicated in the table below. The figures in the table, which relate to presence of metals in the silicon wafer surface after the polishing, are given as the number of atoms/cm^2

Metal	Metal content in the wafer surface after polishing according to the invention	Metal content in the reference wafer surface after polishing
Ti	$0.6 \cdot 10^{10}$	$0.7 \cdot 10^{10}$
Cr	$<0.2 \cdot 10^{10}$	$2 \cdot 10^{10}$
Fe	$0.5 \cdot 10^{10}$	$1 \cdot 10^{10}$
Ni	$1 \cdot 10^{10}$	$2 \cdot 10^{10}$
Cu	$5 \cdot 10^{10}$	$9 \cdot 10^{10}$
Al	$0.4 \cdot 10^{10}$	$2 \cdot 10^{10}$
Na	$6 \cdot 10^{10}$	$8 \cdot 10^{10}$

Evidently, metal contamination of the wafer surface as polished is clearly lessened by the present invention.

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Claims

1. Use of a complexing agent in a composition comprising amorphous silica for chemical mechanical polishing of a semiconductor substrate, for the purpose of avoiding metal contamination of said semiconductor substrate.

2. Use according to claim 2, c h a r a c t e r i s e d in that the complexing agent is NH_4OH.

3. A composition for chemical mechanical polishing of semiconductor substrates, which composition contains amorphous silica and ammonium ions, c h a r a c t e r i s e d in that the composition comprises a sequestering agent.

4. A composition according to claim 3, c h a r a c t e r i s e d in that the sequestering agent is a chelating agent.

5. A composition according to claim 4, c h a r a c t e r i s e d in that the chelating agent comprises a plurality of substituted acetic acid groups.

6. A composition according to claim 5, c h a r a c t e r i s e d in that the chelating agent is a EDTA, DTPA, HEDTA, NTA, or a combination thereof.

7. A composition according to any one of claims 3 - 6, c h a r a c t e r i s e d in that the silica is colloidal.

8. A method for chemical mechanical polishing of a semiconductor substrate, c h a r a c t e r i s e d in that a composition according to any of claims 3 - 7 is used to polish said substrate.

9. A method according to claim 8, c h a r a c t e r i s e d in that the method is a chemical mechanical planarization method.

10. A method according to claim 8 or 9, c h a r a c t e r i s e d in that said semiconductor is Si, GaAs, InP, or Ge

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 C09K3/14 C09G1/02 H01L21/321

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 C09K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DATABASE WPI Section Ch, Week 8851 Derwent Publications Ltd., London, GB; Class A97, AN 88-363748 XP002100340 & JP 63 272460 A (MITSUBISHI MONSANTO KK) , 9 November 1988 see abstract ---	1,3-10
X	US 4 954 142 A (CARR JEFFREY W ET AL) 4 September 1990 see column 3, line 31 - line 66; examples 1-4 ---	1,3-10
X	US 4 462 188 A (PAYNE CHARLES C) 31 July 1984 see table 1 --- -/--	1,3,4, 7-10

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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